IN THE CLAIMS

11. (Previously Amended) A p-channel metal-oxide-semiconductor transistor, comprising:

a silicon substrate;

a silicon dioxide (SiO2) gate oxide, coupled to the substrate;

a gate, coupled to the SiO2 gate oxide;

source/drain regions formed in the substrate on opposite sides of the gate; and

a Si1-xGex channel region, having a germanium molar fraction x, located underneath the SiO2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the Si1-xGex channel region forms a continuous Si1-xGex/SiO2 gate oxide interface wherein no germanium oxide is present at the Si1-xGex/SiO2 gate oxide interface as a result of ion implantation of germanium through the previously formed SiO2 gate oxide.

12. (Previously Canceled)

13. (Original) The transistor of claim 11, wherein the Si1-xGex channel is approximately 100 to 1,000 angstroms thick.

14. (Original) The transistor of claim 11, wherein the molar fraction of germanium is approximately 0.2.

24. (Previously Amended) A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising:

a Si1-xGex channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO2) gate oxide and between a source region and a drain region;

wherein x is less than or equal to 0.6, and wherein the Si1-xGex channel region forms a continuous Si1-xGex/SiO2 gate oxide interface wherein no germanium oxide is present at the Si1-xGex/SiO2 gate oxide interface as a result of ion implantation of germanium through the previously formed SiO2 gate oxide.

25. (Previously Amended) A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising: SiO2

a Si1-xGex channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO2) gate oxide and between a source region and a drain region, wherein x is less than or equal to 0.6, and wherein the Si1-xGex channel region forms a continuous Si1-xGex/SiO2 gate oxide interface wherein no germanium oxide is present at the Si1-xGex/SiO2 gate oxide interface as a result of ion implantation of germanium through the previously formed SiO2 gate oxide; and

wherein the Si1-xGex channel region is formed from ion implanting germanium (Ge) into the substrate at a dose of approximately 2 X 1016 atoms/cm2, and wherein the Ge is implanted at an energy of approximately 20 to 100 keV.

26. (Previously Amended) The transistor of claim 24, wherein the Ge is dispersed in the substrate to a depth of approximately 100 to 1,000 angstroms.

27. (Previously Amended) The transistor of claim 24, wherein the Ge is dispersed in the substrate to a depth of approximately 300 angstroms.

28. (Previously Amended) A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising:

a Si1-xGex channel region, having a germanium molar fraction of 0.2, and formed in the substrate, underneath a silicon dioxide (SiO2) gate oxide and between a source region and a drain region, wherein the Si1-xGex channel region forms a continuous Si1-xGex/SiO2 gate oxide interface wherein no germanium oxide is present at the Si1-xGex/SiO2 gate oxide interface as a result of ion implantation of germanium through the previously formed SiO2 gate oxide.

29-31. (Previously Canceled)

32. (Previously Amended) The transistor of claim 28, wherein, the Si1-xGex channel region was formed by a process comprising:

ion implanting Ge ions through the gate oxide on the substrate at a dose of approximately 2 X 1016 atoms/cm2, and wherein the Ge was implanted at an energy of approximately 20 to 100 keV; and

annealing the substrate in a furnace at a temperature of approximately 450 to 700 degrees Celsius.

33-37. (Previously Canceled)

38. (Previously Amended) A semiconductor transistor, comprising:

a silicon substrate;

a silicon dioxide (SiO2) gate oxide, coupled to the substrate;

a gate, coupled to the SiO2 gate oxide;

source/drain regions formed in the substrate on opposite sides of the gate; and

a Si1-xGex channel region, having a germanium molar fraction of x, and located underneath the SiO2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the Si1-xGex channel region forms a continuous Si1-xGex/SiO2 gate oxide interface wherein no germanium oxide is present at the Si1-xGex/SiO2 gate oxide interface as a result of ion implantation of germanium through the previously formed SiO2 gate oxide.

39. (Previously Amended) The transistor of claim 38, wherein the Si1-xGex channel is approximately 100 to 1,000 angstroms thick.

40. (Previously Amended) A semiconductor transistor formed on a silicon substrate, comprising:

a Si1-xGex channel region, having a germanium molar fraction of 0.2 formed in the substrate, underneath a silicon dioxide (SiO2) gate oxide and between a source region and a drain region, wherein the Si1-xGex channel region forms a continuous Si1-xGex/SiO2 gate oxide interface wherein no germanium oxide is present at the Si1-xGex/SiO2 gate oxide interface as a result of ion implantation of germanium through the previously formed SiO2 gate oxide.

41. (Previously Amended) A semiconductor transistor formed on a silicon substrate, comprising:

a Si1-xGex channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO2) gate oxide and between a source region and a drain region, wherein x is less than or equal to 0.6, and wherein the Si1-xGex channel region forms a continuous Si1-xGex/SiO2 gate oxide interface wherein no germanium oxide is present at the Si1-xGex/SiO2 gate oxide interface as a result of ion implantation of germanium through the previously formed SiO2 gate oxide; and

wherein the Si1-xGex channel region is formed from ion implanting germanium (Ge) into the substrate at a dose of approximately 2 X 1016 atoms/cm2, and wherein the Ge is implanted at an energy of approximately 20 to 100 keV.

42. (Previously Added) The transistor of claim 41, wherein the Ge is dispersed in the substrate to a depth of approximately 100 to 1,000 angstroms.

43. (Previously Amended) The transistor of claim 41, wherein the Ge is dispersed in the substrate to a depth of approximately 300 angstroms and the germanium molar fraction is about 0.4.